

# Thermal Cycling and ESD Evaluation of Embedded Resistors and Capacitors in PWB

Jiming Zhou, John D. Myers, Graeme R. Dickinson  
Delphi Delco Electronics Systems, P.O. Box 9005, Kokomo, IN, 46904-9005

## Abstract

Embedded capacitors and resistors have great potentials for high frequency, high density, and low cost applications. Delphi Delco Electronics Systems has been involved in technology development activities for embedded passives since 1996. This paper summarizes the current results of materials evaluation for the Advanced Embedded Passives Technology (AEPT) project. Test vehicles were designed to evaluate embedded capacitor and resistor technology. Thermal cycling (-40 to 125 °C, 1h/cycle, 1000 cycles) and electrostatic discharge (ESD,  $\pm 2$ ,  $\pm 4$ ,  $\pm 6$ , and  $\pm 8$  kV) tests were conducted on six resistive and five capacitive materials respectively. The test results are discussed. It is believed that thermally and electrically stable resistive material with broad resistance values (e. g. 10 to  $1M\Omega/\text{sq.}$ ) and capacitive material with high capacitance density (e.g. 200 nF/in<sup>2</sup>) are the key factors in moving embedded passives from a niche market to a broad base of applications.

## Introduction

The concept of embedded passives technology (EPT) is to fabricate passives such as resistors and capacitors into printed wiring boards (PWBs) during the board fabrication process. Compared with integrated passives, which consist of passive arrays and networks on carrier substrates, embedded passives are relatively recent [1 - 4]. The embedded passive technology is driven by multiple factors such as the need for better electrical performance, higher packaging density, and potential cost saving. Using this technology, passives may be placed directly below active devices (ICs). The shorter distance between the passives and active components reduces the parasitics associated with surface mounted passives, resulting in better signal transmission and less cross talk. Lower loss and lower noise yield better electrical performance, especially at high frequencies. Furthermore, passives can be 80 to 95% of the total number of components and consume up to 40 % of the surface area of PWBs. By reducing the number of surface mount passive components, PWB real estate is freed, thereby allowing higher packaging densities to be achieved. Additionally, the potential for lower material costs exists by reducing the amount of discrete passives, flux, and solder used. Embedded technology can also simplify the assembly process and reduce assembly cost especially when 0201 components have to be used. The combination of the material and assembly process savings using embedded passives can eventually reduce the overall product cost compared with the utilization of SMT discrete passives.

Both thick film, and thin film technologies exist for the application of resistive and dielectric materials

into PWB's. Thick film technology involves the screen printing of a dielectric or resistive paste onto copper foil. Thick film printing is a fast process; however passives made this way are not as small and uniform as passives made using thin film processing. Thin film is deposited on copper by processes such as plating, sputtering or vapor deposition. Good uniformity and small size can be achieved using thin film application methods [2]. However, thin film application of resistive and dielectric materials is more expensive than the thick film counterparts and thin films cause material handling problems for the board fabricator which also leads to higher cost.

Delphi Delco Electronics Systems has been involved in embedded passive technology in PWB since 1996 as a member of a consortium investigating ink jetted resistors and, in 1998, Delphi participated in the Embedded Distributed Capacitance (EDC) consortium. This was followed by involvement in a consortium investigation of both resistors and capacitors called the Advanced Embedded Passives Technology (AEPT) in 1999. The AEPT consortium consists of materials suppliers, board fabricators, process equipment manufacturers, a CAD tool company, a cost assessment software developer, and several original equipment manufacturers (OEMs). These companies represent every aspect associated with the technology development.

The goal of the consortium is to develop and validate thermally and electrically stable resistive materials that can cover a large range of resistance values from 10  $\Omega/\text{sq.}$  to  $1M\Omega/\text{sq.}$  and dielectric materials that can reach a capacitance of 200 nF/sq. in.. In order to evaluate materials and board fabrication processes for

use with embedded capacitors and resistors, Delphi Delco designed the vehicles for testing of both embedded capacitors and resistors. Thermal cycling, humidity, thermal shock, mechanical bending, electrostatic discharging (ESD), thermal coefficient of resistance (TCR), and thermal coefficient of capacitance (TCC) tests were conducted by material suppliers and OEMs. Five materials were evaluated for use as embedded capacitors, and six materials were evaluated for use as embedded resistors. In this paper, the testing results of thermal cycling and ESD are reported.

**Materials and Test Vehicle**

A comparison of surface mount technology (SMT) and embedded passive technology (EPT) are shown in Figure 1. The resistor test vehicles contained five arrays of resistors. There were generally four rows of nine resistors per array. Each row varied the spacing between the terminations of the resistive material, as well as the widths of the copper terminations. 5, 10, 20, 40, and 50 mil spacings were tested with copper terminations varying from 5 to 20 mils. The variations of resistor configurations are shown in Fig. 2. Although the area of resistive material printed in the PWB for each resistor was rectangular, the area between the contacts was always a square. The different sizes of resistors (squares) and terminations were designed to test reliability, stability, and process capability of embedded passives. Although some daisy-chained resistors were tested, only the testing results for single resistors are reported in this paper.

The capacitor test vehicles contained an array of 80 small capacitors, and an array of six larger capacitors, for a total of 86 embedded capacitors. The configuration of a single capacitor can be seen in Fig. 3. Each capacitor has the power terminal routed to the connector by means of a plated through hole (PTH) at the center of the capacitor. For the 1x6 array, a 13.5 mil hole was drilled with an antipad of 33.5 mils in layer 3. For the 4x20 array, four hole sizes and four antipad annuli in the ground plane were used in 16 hole/annulus combinations to investigate their impact on board fabricating process and reliability. The four hole sizes were 10, 13.5, 16.5, and 20 mils, and the four annular radii were 6, 8, 10, and 12 mils respectively [3].

The test boards were fabricated by several board fabricators. OhmegaPly™ and BC2000™ were chosen as benchmarks for resistor and capacitor materials respectively since they have been on the market for a long time as embedded passive materials. Both materials are thermally and electrically stable. The disadvantage of these materials are their low resistance ( $\approx 50 \Omega/\text{sq.}$ ) and low capacitance ( $\approx 1 \text{ nF}/\text{sq. in.}$ ) resulting in large board areas for high-value ohm resistors or high-

value capacitors. The AEPT consortium is seeking materials with a broad range of resistance values and dielectrics which can be used to create higher capacitance densities. To protect material supplier's technical and business information, resistor materials are designated as R1, R2, R3, R4, and R5 except benchmark OhmegaPly™. Capacitor materials are designated as C1, C2, C3, and C4 except benchmark BC2000™. The R4 resistive material has two resistive values,  $100 \Omega/\text{sq.}$  and  $10 \text{ k}\Omega/\text{sq.}$ , designated as R4-100 and R4-10k. The C4 has two dielectric material thicknesses,  $4 \mu\text{m}$  and  $8 \mu\text{m}$ , designated as C4-4 and C4-8 respectively.

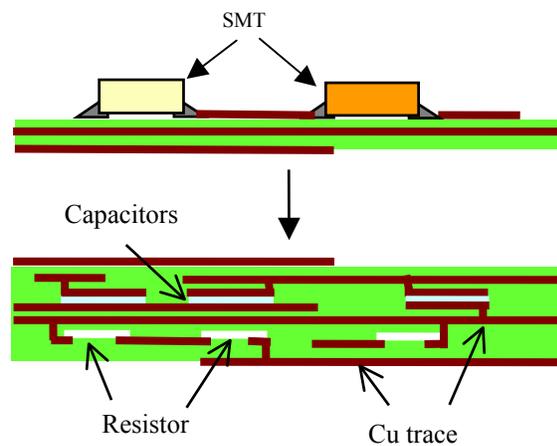


Fig. 1 From SMT to EPT.

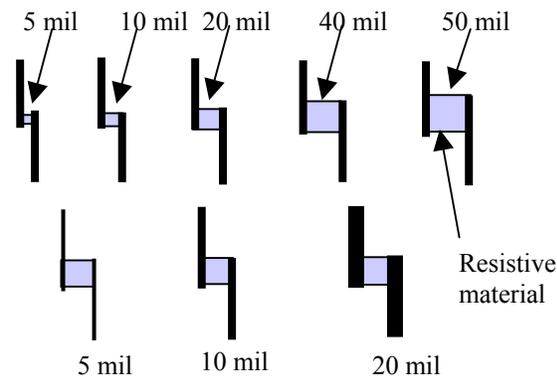
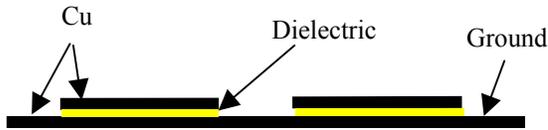


Fig. 2 The embedded resistors have different sizes (5, 10, 20, 40, and 50 mil square) and the copper terminations have 5, 10, and 20 mil size.



**Fig. 3** Cross-section of the tested capacitors that share a common ground plane.

### Testing

#### Conditioning

Each capacitor and resistor board first was subjected to a bake at 85°C for 24 hours to eliminate the possible influence of moisture absorption. Then, the boards were measured to establish the base line set of data used for further comparison. Resistor boards were tested at room temperature by using a Fluke 8050A digital multimeter. Capacitors were measured using a HP 4284 precision LCR meter. Three parameters, capacitance (C), dissipation factor ( $D_f$ ), and parallel resistance ( $R_p$ ), were collected simultaneously at 1kHz and 1V testing condition for each capacitor.

#### Reflow and Thermal Cycle

The boards then underwent three reflow cycles at a peak temperature of 230°C using an Electrovert ATMOS 2000 CR reflow furnace. Three reflow cycles were used to simulate wave soldering, reflow, and reworking steps that the passives would experience during typical board assembly processing. Resistance and capacitance readings were once again recorded at room temperature.

Subsequently, resistor and capacitor boards underwent thermal cycle testing from -40°C to 125°C. The programmed thermal cycle is one hour per cycle with ramp and dwell time of 15 minutes. The actual dwell times were approximately 7 minutes due to thermal inertia. The thermal cycle test was run for 1000 hours with capacitance and resistance measurements taken at room temperature periodically.

#### ESD Discharge

Electrostatic discharging (ESD) was conducted for both resistor and capacitor boards after conditioning. The testing was performed using human body model (HBM, AEC-Q200) and direct contact discharge voltages of  $\pm 2$ ,  $\pm 4$ ,  $\pm 6$ , and  $\pm 8$  kV. Immediately after ESD testing, readings of the resistor and capacitor boards were taken at room temperature using the testing methods described previously.

## Results and Discussions

### Resistor Boards

#### Thermal Cycle

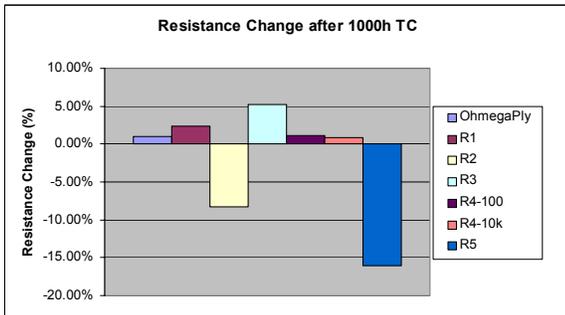
The original resistance data for the six tested materials (boards) are shown in Table 1. Note the 5 mil square data is not displayed because there were high numbers of initial opens and wide variation in values compared to the larger sizes. In general the larger the resistor's physical size the fewer opens and the lower the process variation. This effect was more predominant on thick film resistors than on thin film resistors. The original AEPT goal for process (fabrication) related resistance tolerance was  $\pm 10\%$  without trimming. Data in table 1 indicate that only a few of the material including benchmark OhmegaPly™ can reach this requirement. Electro Scientific Industries (ESI), a member of AEPT, is developing the equipment to trim resistors. Preliminary results show that the embedded resistors on laminate are trimmable and the equipment capable of two percent trim accuracy will be feasible soon [5]. The resistance changes after 1000 hours of thermal cycling can be seen in Figure 4. Benchmark OhmegaPly™, R1, and R4, have resistance changes less than the  $\pm 5\%$ , which is the AEPT target life cycle resistance change. The other materials are thermally sensitive. No thermal cycle induced failures were observed in all the tested materials.

#### ESD

The resistance changes after an 8kV discharge for each material can be seen in Table 2. OhmegaPly™, R1, and R4-100 are ESD stable throughout the testing voltage range from 2 kV to 8 kV. Other materials exhibit resistance change, which is voltage and size dependent with higher voltage creating large resistance drift and larger sizes resulting in less resistance drift. No ESD test was conducted on R5 since it was thermally unstable and the material was dropped from AEPT program.

**Table 1** Initial resistance data.

Resistor size		10 mil	20 mil	40 mil	50 mil
R1	Average $\Omega$ /sq	13.37	15.12	15.77	14.80
	% std. dev.	14.28	22.67	19.35	17.43
R2	Average $\Omega$ /sq	58.32	62.23	59.74	60.46
	% std. dev.	6.98	17.28	12.74	12.72
Ohmega Ply™	Average $\Omega$ /sq	49.60	25.93	37.94	40.17
	% std. dev.	4.81	5.51	3.23	3.01
R3	Average $\Omega$ /sq	115.1	70.42	53.09	54.40
	% std. dev.	29.62	13.23	8.85	12.94
R4-100	Average $\Omega$ /sq	141.5	105.0	96.7	91.30
	% std. dev.	18.7	17.5	7.9	9.2
R4-10K	Average $k\Omega$ /sq	26.8	14.1	11.2	10.40
	% std. dev.	16.8	8.2	8.5	3.8
R5	Average $\Omega$ /sq	80.7	69.4	63.0	54.8
	% std. dev.	19.7	11.7	9.6	6.3



**Fig. 4** Average resistance change for all sizes, after 1000 hour thermal cycling.

**Table 2** Resistance change after 8 kV ESD discharge (%).

	R1	R2	Omega Ply	R3	R4-100	R4-10k
10 mil	-0.08	8.71	0.10	27.63	-2.20	49.58
20 mil	0.0	2.53	-0.51	18.52	1.32	37.79
40 mil	0.08	1.33	-0.37	7.14	0.66	21.71
50 mil	0.09	0.80	-1.26	5.83	0.33	19.69

### Capacitor Boards

#### Thermal Cycle

Three parameters, capacitance, dissipation factor, and parallel resistance, were tested for embedded capacitors before and after thermal cycle and ESD tests. The original capacitance data for the five tested materials (boards) are shown in Table 3. Testing results indicate that the tolerance can be controlled within 5%. Trimming of the capacitors is under consideration depending on tolerance requirement, board fabrication process control, and equipment development. The capacitance change with thermal cycling time can be seen in Figure 5. The capacitance change of all tested materials after 1000 hours of thermal cycling is smaller than 5% which is the target of the AEPT consortium. In fact, the capacitance drifts of C1, C2, and C4 are smaller than that of the benchmark BC2000™. C3 has similar thermal properties but the data are not shown in the figure. No capacitor failures were observed after thermal cycling.

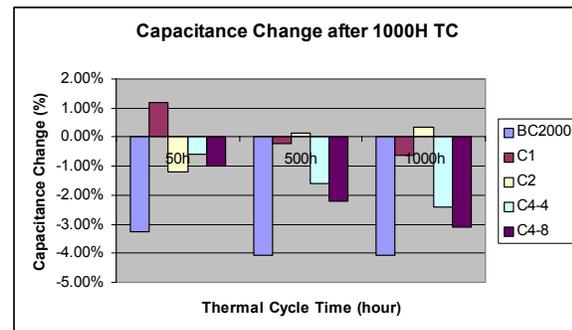
#### ESD

After ESD discharge, the capacitance values changed very little regardless of whether the dissipation factor or parallel resistance changed dramatically. Therefore, the criterion for a capacitor failure is defined as significant parallel resistance change (e.g. from 50MΩ to 1kΩ) and dissipation factor change (e.g. from 0.007 to 10). The number of failures after ESD discharge is shown in Table 4. C1, C4-8, and

the benchmark BC2000™ had zero failures and had dissipation factor changes of less than 1% after ESD discharge. These materials are ESD stable. C4-8 material has a capacitance density nearly 15 times higher than that of the benchmark BC2000. This is a significant improvement in capacitive material development. Others had numerous failures after ESD discharge. The dissipation factor ( $D_f$ ) drift in the last column shows the degree of dissipation factor change of only the capacitors that did not fail. Both the damaged capacitor number and resistance value drift is discharge voltage dependent. Higher discharge voltage results in a higher percentage of capacitors that are damaged. The parallel resistance changes for each discharge voltage tests can be seen in Fig. 6.

**Table 3** Original capacitance data.

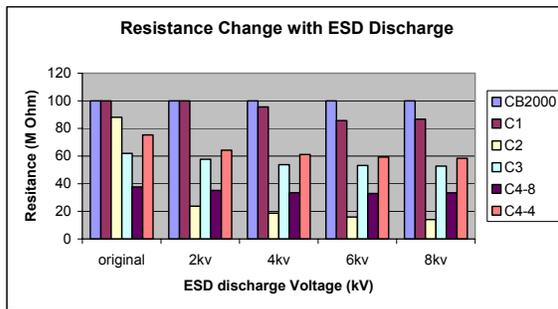
	C1	BC 2000	C2	C3	C4-8	C4-4
Average (pF)	91	24	160	396	373	612
Std. Dev. (pF)	2.8	1.9	3.8	7.7	11.2	8.5
% of Std. Dev.	3.1	7.9	2.4	2.0	3.0	1.4
Cap/sq. in. (nF)	3.3	0.87	5.8	14.2	13.4	22.0



**Fig. 5** Capacitance change after 1000 hours of thermal cycle.

**Table 4** Number of failures after ESD testing. High capacitance materials show easier to be damaged by ESD discharge since the materials have smaller thickness. The dissipation factor ( $D_f$ ) drift in the last column is not for the damaged capacitors. It shows the degree of dissipation factor change of the undamaged capacitors.

	2kV	4kV	6kV	8kV	Total	Av. Cap (pF)	$D_f$ drift after ESD (%)
C1	0/20	0/24	0/25	0/25	0/94	91	<2%
C2	1/25	0/25	4/25	7/25	12/100	160	>6%
BC 2000	0/20	0/25	0/25	0/25	0/95	25	<1%
C3	0/25	1/23	2/25	4/24	7/97	395	<1%
C4-4	3/24	9/24	7/24	17/24	36/96	612	<1%
C4-8	0/8	0/8	0/8	0/8	0/32	373	<1%



**Fig. 6** Parallel resistance changes of capacitor boards after ESD discharging.

### Discussions

The resistive material benchmark OhmegaPly™ is thermally and electrically stable after thermal cycle and ESD tests. However, its value per square is low making it difficult to replace more than a small number of SMT resistors. Most of the tested materials have a similar value range of 50 Ω/sq. So far, only R4 has both 100 Ω/sq. and 10k Ω/sq. material available. Materials with 1 kΩ/sq. and 50 kΩ/sq. are under development and may be available at a later time. Due to fabrication, reliability and trimability issues, resistors ≥ 20 x 20 mil in size are recommended at this development stage. Embedded resistor's ESD withstanding property and power dissipation are size related. Therefore, depending on the requirements of power dissipation and ESD withstand, a larger resistor size may be needed. More data is needed to establish the complete design guideline.

The capacitor material benchmark BC2000™ is thermally and electrically stable. However, its capacitance is only about 1 nF/sq. in. All alternative materials evaluated here have higher values but are still not high enough to replace a significant number of capacitors on a typical mixed signal product. Currently, the C4 material can realize 22 nF/sq. in., which is much higher than that of the benchmark material. The ESD withstanding property of embedded capacitors are discharge voltage related. Depending on the requirement of ESD withstanding, different thicknesses of dielectric material need to be considered. A dielectric, which results in a higher capacitance value per square inch, is expected to be available soon.

A significant impact of embedded passives technology is to shift the manufacturing of passives from component suppliers to board fabricators. Embedded passives inherently make PWB designs more complicated and increase production costs. With the development of CAD tools for embedded passive board design and the establishment of the material standard, the technology is ready for organic

laminare board fabricators to play a more important role in development of the new technology.

### Conclusions

Significant progress in the development of resistance and capacitance materials has been achieved during past six months. Capacitor material with 22 nF/sq. in. and resistance materials with 100Ω/sq. and 10 kΩ/sq. are available. Higher density capacitors and higher Ω/sq. resistors will be in the testing program soon. Many materials are thermally stable, however, only a few materials, including R4-100 and C4-8, are ESD insensitive. Better CAD software, material specifications, and fabricator availability are expected soon.

The original benchmark materials were primarily used for computer backplanes. It appears that the new materials discussed here allow a broader application of the technology than was possible with the benchmark materials. However, new materials, which allow even higher package density, will be needed to reach the main stream market. It is believed that thermally and electrically stable resistive materials with broad resistance values (e. g. 10 to 1MΩ/sq.) and capacitor materials with high capacitance density (e.g. 200 nF/in<sup>2</sup>) are the key factors in moving embedded passives from a niche market to a broad base of applications. The current materials under development have applications in high frequency, high speed computers, portable, and wireless designs. The next generation of materials which meet the cost/performance requirements of the market are just around the corner. So, stay tuned.

### Acknowledgement

This NCMS/AEPT Consortium work is performed under support of Delphi Automotive Systems and the U.S. Department of Commerce, National Institute of Standards and Technology, Advanced Technology Program, Cooperative Agreement Number 70NANB8H4025. The authors would like to thank Mark A. Kelly for his ESD testing assistance.

### References

1. J. Peiffer, "Embedded Capacitor Material Evaluation", pp1-4, AT2-2, IPC SMEMA Council APEX 2001
2. J. Wang and S. Clouser, "Thin Film Embedded Resistors", p7, IPC Review, June 2001
3. P. Bowles, "Reliability Evaluation of Embedded Decoupling Capacitance", pp1-8, AT2-3, IPC SMEMA Council APEX 2001
4. J. Prymak, S. Bhattacharya, K. Paik, Fundamentals of Passives: Discrete, Integrated, and Embedded, "Fundamentals of Microsystems Packaging", Ed. By R. R. Tummala, McGraw-Hill 2001
5. AEPT Ninth Quarter Program Report (Feb. 2001 to April 2001), 2001